FAST, ACCURATE, ON-WAFER EXTRACTION OF PARASITIC RESISTANCES AND INDUCTANCES IN GaAs MESFETs AND HEMTs

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ABSTRACT

A novel method of extracting the parasitic resistance and inductance values for MESFETs and HEMTs is presented. The technique requires the use of only rf two-port measurement data (ie. s-parameters), is extremely accurate, straightforward to implement and works equally well for both MESFETs and HEMTs. The technique makes use of "cold-chip" measurements in conjunction with a unique analysis that has proven to be both fast and robust.

INTRODUCTION

In order to extract small-signal equivalent circuit elements from s-parameter data of FETs, a technique is needed to initially extract the drain, gate and source parasitic resistances and inductances. Once these parasitics have been obtained, the rest of the circuit elements can be directly extracted by manipulation of the deembeded s-parameter data.[1] The technique described in this paper is currently implemented as part of an automated on-wafer RF characterization system which extracts small-signal models in real-time for different DC biases and provides statistical parameter information for GaAs devices fabricated at Motorola. When appropriate bias and network analyzer equipment are utilized, the system is capable of placing the probes, making DC and microwave measurements, and computing intrinsic model element values of a device in approximately 20 seconds. In order to optimally exploit this capability, it is necessary to use a complementary fast and accurate parasitic extraction technique. The technique described in this paper makes use of "cold-chip" measurements in conjunction with a unique analysis that has proven to be both fast and robust. Because the technique extracts the parasitic elements from microwave measurement data, low frequency dispersion problems associated with parasitic resistances are also avoided.

The speed and generality constraints imposed by the application described above eliminate many of the parasitic extraction methods suggested in the literature. Some of the more traditional methods obtain the parasitic resistances from DC measurements alone and involve the use of complex extraction algorithms and optimizations which, despite being accurate, are not suitable for implementation in a fast on-wafer characterization system described above.(See for example [2]-[5]) The method suggested in this paper uses small-signal measurements, with the DC value of V_{DS} set to zero and V_{GS} set to a value larger than the Schottky barrier height. Two-port measurements are then taken at increasing V_{GS} biases. The approach used in our work is a different interpretation of the previously reported "cold-FET" techniques.[3] The method described here does not require that channel resistance or diode resistance be evaluated or that excessive values of gate current be used in the measurements.

We initially model the intrinsic distributed gate region of the forward-biased FET with only three resistors, as shown in Fig. 1. The forward-bias applied at the gate-source and gate-drain junctions eliminates the device capacitances CGS and CGD from the measurements, thereby yielding the 2-port Z-parameter equations listed in the figure, where R_{CH} is the channel resistance and R_{GG} is the diode resistance of the Schottky junction. The same model applies equally well to a HEMT, where the value of R_{GG} then includes both the resistances of the Schottky diode and the resistance through the wide bandgap material. The parasitic elements are then extracted as follows:

IF2

INDUCTANCES

The parasitic inductances may be extracted by examining the slope of the imaginary part of the "cold-FET" z-parameters at high frequencies. From the model depicted above, the slopes of the imaginary part of the z-parameters versus frequency f are equal to: $\frac{\Delta Z_{12}}{\Delta f}=2\pi L_S$, $\frac{\Delta Z_{11}}{\Delta f}=2\pi(L_G+L_S)$, and $\frac{\Delta Z_{22}}{\Delta f}=2\pi(L_D+L_S)$. Typically, these values are extracted from the high-frequency slope of the imaginary parts of the z-parameters versus frequency at a given gate bias.

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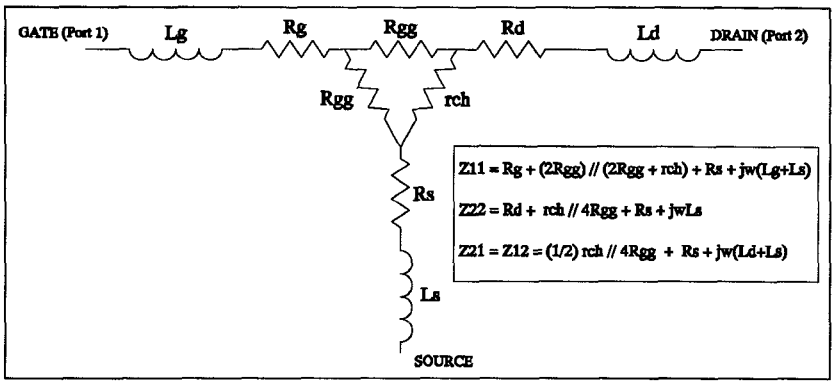

Fig. 1: Small-signal model and 2-port equations of a MESFET with "cold-FET" biasing.

SOLVING FOR PARASITIC RESISTANCES BY A SIMPLE OPTIMIZATION:

The equivalent circuit of Fig. 1 is comprised of three fixed parasitic resistances (R_S, R_D, and R_G) , a voltage dependent channel resistance (R_{CH}) and a voltage dependent channel-to-gate resistance (R_{GG}). Each forward bias measurement provides three unique equations relating these resistance values to the real part of the z-parameters. By utilizing forward bias data made at three distinct V_G bias levels, we are left with nine independent equations (the real parts of three sets of z-parameters) and nine unknowns [R_S, R_D, R_G, $R_{CH}(V_{G1})$, $R_{CH}(V_{G2})$, $R_{CH}(V_{G3})$, $R_{GG}(V_{G1})$, $R_{GG}(V_{G2})$, $R_{GG}(V_{G3})$]. The linearized equations that result for one bias point are given in the Appendix. A solution to the set of equations is easily found using standard linear optimization techniques. One important feature of this technique is that accurate values for parasitic resistances of HEMTs are also achievable. Conventional techniques have not been applicable for HEMT structures since forward biasing the devices produces unwanted resistance in the parasitic MESFET within the device. Using this method, these unwanted resistances are lumped into the values established for R_{GG}. The values determined for the actual parasitic resistances, including R_G, can be used with equivalent circuits to provide excellent agreement with measured s-parameters at all bias levels.

Table 1 presents resistance and inductance values determined for a a 0.7x25 μm AlGaAs/GaAs HEMT. These values were used as part of an equivalent circuit for the devices under normal bias conditions and found to produce excellent agreement with the measured data as shown in Fig. 2. The model data uses the parasitic resistance values obtained using the optimization technique of the previous section, the inductance extraction described above and the direct intrinsic device extraction described previously [1].

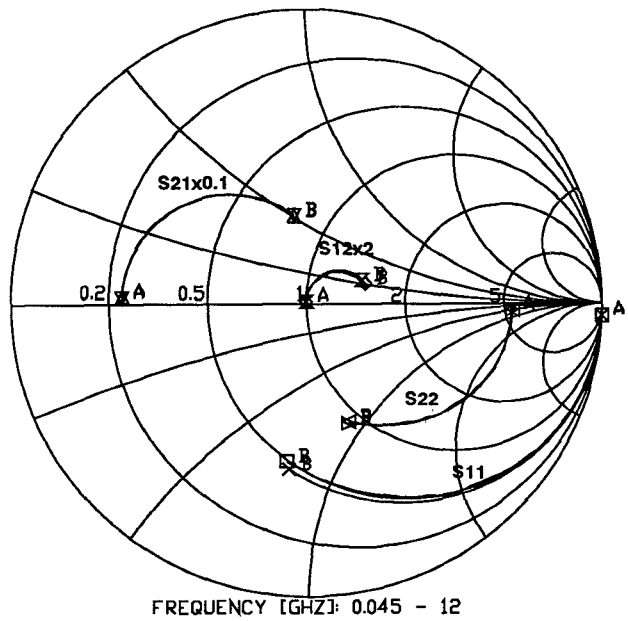

Fig. 2: Measured and Simulated S-parameters of a 0.7x25μm AlGaAs/GaAs HEMT with VDS=2.0 and IDS=25mA. The parasitic resistances were obtained by the optimization extraction method.

TABLE 1. Calculated parasitic resistance values for a GaAs HEMT

DEVICE	Rs (Ω)	Rd (Ω)	Rg (Ω)	Ls (nH)	Ld (nH)	Lg (nH)
0.7x25 μm HEMT	3.08	3.39	18.6	0.00	0.04	0.02

SOLVING FOR MESFET PARASITIC RESISTANCE BY THE DIFFERENTIAL METHOD

For the case of the MESFET, a single assumption concerning the functional form of the value of $R_{GG}(V_G)$ dramatically reduces the computation required to compute parasitic resistance values. The method that results from this assumption eliminates the need for optimization while providing extremely accurate estimates of the parasitic resistance values. This method is particularly suitable for implementation in a fast extraction system because explicit analytical expressions are obtained for the parasitic resistances in terms of the measured microwave data. The basis of the differential method is the assumption that the diode resistance R_{GG} varies with $1/I_G$ (the inverse of the gate current) as $\frac{\Delta R_{GG}}{\Delta 1/I_G} = \frac{d\, nkT/I_G}{d\, 1/I_G} = R_{GG}I_G$ and that the measurements are taken at low gate current levels such that $4R_{GG} >> R_{CH}$. Under these assumptions, it can be shown that the above equations can be simplified to:

$$Z_{11} = ZO_{11} + m_{11}\frac{1}{I_G} = (R_G + R_S) + (R_{GG}I_G)\frac{1}{I_G}, \quad (1)$$

$$Z_{22} = ZO_{22} + m_{22}\frac{1}{I_G} = (R_D + R_S) + \left(\frac{R_{CH}^2 I_G}{4R_{GG}}\right)\frac{1}{I_G}, \quad (2)$$

$$Z_{12} = ZO_{12} + m_{12}\frac{1}{I_G} = R_S + \left(\frac{1}{2}\right)\left(\frac{R_{CH}^2 I_G}{4R_{GG}}\right)\frac{1}{I_G} \quad (3)$$

where m_{11}, m_{22} and m_{12} are the slopes of the linear fits of the Z vs $1/I_G$ data. Fig. 3 illustrates the validity of the above assumptions for a 1.0x250 μm GaAs recessed-gate MESFET.

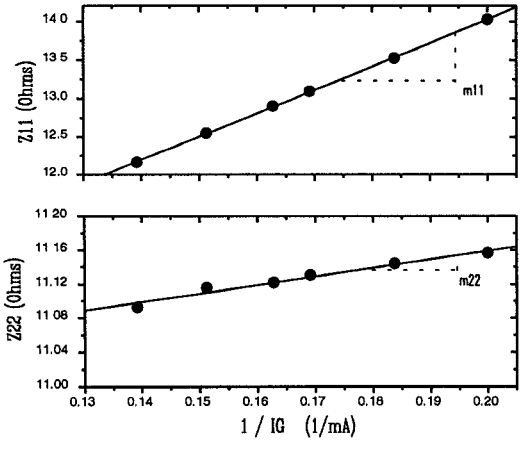

Fig. 3: Measured Z11 and Z22 versus 1/IG for a 1.0x250 μm GaAs MESFET biased in the "cold-FET" regime, measured at 500MHZ. The slopes of the least-squares fit can be shown to be m11=RggIG and $m22=\left(\frac{rch^2 IG}{4Rgg}\right)$.

The differential extraction procedure then involves 1) setting closely-spaced gate currents, 2)measuring the z-parameters, and 3)computing the derivatives m_{11} and m_{22} (m_{12} is half of m22, so its extraction is not necessary). The parasitic resistances can then be directly extracted from the above equations . For our on-wafer extraction system, we typically employ only two-bias points, at a current level of less than 10mA/mm. Table 2 depicts the parasitic elements as extracted from a 1x250 μm gate GaAs MESFET:

With the parasitic resistances and inductances determined by the above methods, the other circuit elements of a small-signal FET model were extracted by a previously described technique.[1] The excellent agreement between measured and simulated data for the on-wafer extraction algorithm using the differential method is depicted in Fig. 4.

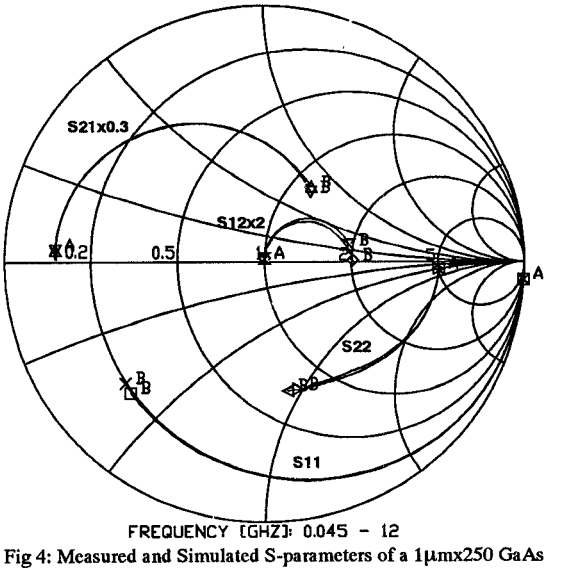

Fig 4: Measured and Simulated S-parameters of a 1μmx250 GaAs MESFET obtained from the on-wafer characterization system using the differential "cold-FET" measurement."

ACCURACY AND LIMITATIONS

The basis of the proposed model lies in the assumption that the forward-bias employed in the measurement is large enough to cause the depletion region under the gate of the FET to disappear, thereby eliminating the device capacitances C_{GS} and C_{GD} from the model. This assumption can be easily checked by monitoring the phase of the low-frequency s-parameters versus bias and checking that it is indeed negligible with respect to its magnitude. We have observed that this assumption does not hold true for MESFET lots which exhibit abnormally high parasitic gate resistances which severely limit the forward bias current. Typically, m_{11} (the slope of z_{11} versus $1/I_G$) is easily measured by a simple least-squares fit, whereas m_{22} , due to its much smaller magnitude, requires some averaging of the first few z-parameters to be sufficiently accurate. For a typical GaAs MESFET, the differential technique proposed in the paper generally yields extraction errors in the range between 5 and 10% between measured and extracted s-parameter data.

TABLE 2 : Extraction of parasitic resistances of a GaAs MESFET by the Differential Method

Ig (mA)	z11 (Ω)	z12 (Ω)	z22 (Ω)	$\frac{\Delta z_{11}}{\Delta 1/Ig}$ Ω mA	$\frac{\Delta z_{22}}{\Delta 1/Ig}$ Ω/mA	2*Rgg (Ω)	rch (Ω)	Rs (Ω)	Rd (Ω)	Rg (Ω)
5	14.021	5.4875	11.156	30.6618	0.8036	12.265	1.975	4.57	4.89	2.86
5.44	13.525	5.472	11.143			11.273	1.830	4.62	4.84	2.85

CONCLUSION

A novel method of extracting the parasitic resistance and inductance values for MESFETs and HEMTs suitable for use in an automated on-wafer parameter extraction system, was demonstrated . The technique requires the use of only rf two-port measurement data (ie. s-parameters), is accurate, straightforward to implement and works equally well for both MESFETs and HEMTs. The technique makes use of forward biased "cold-chip" measurements in conjunction with a unique simplified analysis that has proven to be both fast and robust.

APPENDIX

With the assumptions used in the model of Fig. 1, the following equations can be derived for a single bias condition:

$$\mathrm{Re}[Z_{11}] = R_S + R_G + R_A(V_G) + R_B(V_G) \qquad (A.1)$$

$$\mathrm{Re}[Z_{12}] = R_S + R_A(V_G) \qquad (A.2)$$

$$\mathrm{Re}[Z_{22}] = R_S + R_D + 2R_A(V_G) \qquad (A.3)$$

where

$$R_A(V_G) = \frac{2R_{GG}(V_G)R_{CH}(V_G)}{R_{CH}(V_G) + 4R_{GG}(V_G)} \qquad (A.4)$$

$$R_B(V_G) = \frac{4R_{GG}^2(V_G)}{R_{CH}(V_G) + 4R_{GG}(V_G)} \qquad (A.4)$$

Additional bias levels provide the additional equations per bias level corresponding to equations A(1) - A(3), where the values of R_A and R_B are distinct for each bias setting.

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